# MEMORANDUM

To: AA+ group
From: George Robbins
Subject: Low End Chipset (AA+) Roadmap
Date: Wed Dec 4 09:02:35 EST 1991

This document is intended to describe, from the systems point of view, the requirements of a low end amiga chipset and a realistic short/long term plan of developing and implementing such a chipset.

## Background:

Development work to date has resulted in an enhanced version of the Amiga chipset (AA) that represents an considerable improvment in the capabilities of the Amiga system, however additional work is needed to integrate this chipset for cost-effective use in low end products and move the chipset to an non-proprietary, low power technology.

Management approval has been obtained for a development effort and an extremely aggressive timetable has been proposed for an (as yet) poorly defined development effort.

I am concerned that we not take care that we do not sacrifice either support for short term needs, nor progress towards longer term product requirements and competitive position in the name of what is effectively a near term corporate cost reduction project.

I am also concerned that we take care to partition this new chipset in a way that allows for a maximum of systems flexibility so that chipset "fits" in whatever systems we are designing when the new chipset is completed and can be modified to suit minor changes in the system environment without requiring major effort on the part of the LSI design and test engineering groups.

## Overview:

In view of the above, I suggest a three phase approach that yields short term benefits to insure design flexibility while the new chipset is being developed, provide a clear basis for development of the new chipset and define the next step beyond the current effort so that architecture and compatibility needs are which might impinge on the current effort are well understood.

## Phase 0:

Phase 0 is intended to harvest the yield of the development efforts to date in a usable form and provide a secure basis for any "AA" system implementations undertaken while the new chipset is under development.

Phase 0 consists of two minor LSI development tasks and two optional tasks that could be done by either LSI development or systems.

It is intended that the LSI development tasks overlap the architectural portion of the Phase 1 tasks.

Task 1 - 100 pin Agnus

Modification of the current NMOS Alice design to provide a universal Agnus/Alice chip in a 100-pin surface mount package. This device includes a processor interface compatible with either 16 or 32 bit processors, supports either 16 or 32 bit memory busses and eliminates external TTL currently needed for clock switching and DRAM decode. No "architectural" enhancements are involved, however some minor core changes to extend exiting capabilities are detailed below.

Task 2 - Paula MIDI/FIFO

Modification to the existing Paula chip to provide additional FIFO stages in the UART function to resolve the current "MIDI" high-baud rate thruput problems.

Task 3 - Gate Array Paula Implementation (optional)

The current Paula chip is reimplemented in a generic gate array to provide an improved UART function, enhanced (High Density) FDD controller and 16-bit (CD quality) audio function. The FDD and 16-bit audio rely on extension of 32/64-bit memory interface to the Paula chip. Given the generic gate array implementation the Analog Audio DAC output is replaced by a serial interface to a standard CD audio-DAC.

Task 4 - Gate Array 8520 Implementation (optional)

The current custom NMOS 8520 design is converted to a generic gate array to allow integration of the two 8520's and random glue logic into a single package. It is intended that the resulting 8520 modules can be used as macros for combination with other functions and glue logic which might be required in a given implementation.

## Phase 1:

Phase 1 is intended to provide a CMOS implementation of a "AA" equivalent chipset for use in low-end and mid-range systems shipping 18-24 months from now. The core technology is intended to be modular and may be repackaged in several forms over it's effective lifetime.

There are two major tasks delineated, one for LSI design, one in the LSI development area, one which could be done by systems with support from LSI design.

Please note that the partitioning between the two chips remains parallel to what exists today - there are no "processor bus" or system glue functions included in the ADP chip and no "chip bus" functions included in the combined I/O chip.

Task 1 - 144-pin ADP (Agnus, Denise, Paula) Chip

The 100-pin Alice/Agnus design as defined in Phase 0 is combined with the enhanced Paula chip and current Lisa Chip (AA Denise) to provide a single chip which implements the "Amiga" functionality. The baseline design includes a 256x19 bit CLUT with Analog RGB outputs and 32-bit sprites. Layout variations based on the same modular design could provide a 256x25 bit CLUT with either internal or external DAC's and 64-bit sprites, at the expense of either dies size and/or pin count. The Paula function would include the 16-bit audio with external serial CD-DAC described above, support for High Density FDD would be optional.

Task 2 - 144/160-Pin Combined 8520/Glue/Gayle Chip

The gate array 8520 implementation described above is combined the "Gayle" system control functions and random glue logic. If the gate array technology permits the real-time clock and RS232 function can be included. The design is fully modular so the requirements of different systems can be accommodated or different partitioning can be used if a high pin-count gate array is not cost effective.

## Phase 2:

Phase 2 is intended to complete the architectural extensions / performance enhancements needed to maintain the competitive market position of the Amiga based systems. The tasks/features are not fully defined at this point, however the should be defined as part of the architectural component of the Phase 1 work.

Item 1 - Display Capability Enhancements

Basically, this amounts to the addition of 4/8 bit chunky pixels, a 16/24 bit true-color mode and a "HAM" replacement involving a on-the-fly computational/de-compression modality.

Item 2 - Blitter Performance Enhancements

The current Agnus blitter function is enhanced to effectively take advantage of the increased (32/64-bit) bandwidth provided by the AA architecture. This could be done either by increasing the width of the blitter data-paths or by executing multiple 16-bit blitter cycles within the basic memory cycle.

Item 3 - High Density FDD / 16-bit Audio Support

If these functions were not included in either of the two previous phases, they are included as part of this phase.

## Summary:

I think this plan has several benefits. First, it establishes a framework that everyone involved can work with and base their plans on. Second, it establishes longer term goals that can be used a basis for LSI development staffing and equipment acquisition.

Finally, there are some very real benefits associated with the proposed partitioning. First, LSI development is responsible for *one* custom chip design. While there is some pain associated with the "one big chip", it does concentrate all resources on a single entity and problems associated with trying to coordinate design, implementation, test development and debugging of N-chips are avoided. Second, the areas of concern/responsibility for the LSI design and System design areas are clearly delineated. The LSI designers do not have to worry about irrelevant system design issues, the Systems designers have the system interface component available in a plastic form that does not require LSI design involvement for system customization.

Attachments:

I. List of Phase 0 Agnus/Alice Changes

II. List of Phase 2 Architectural Enhancments

## Phase 0 Agnus/Alice Changes

1) 100-pin package includes 16/32-bit processor interface and 16/32 bit memory interface.

2) Addition of FMODE (fetch mode) bits to control enhanced fetch (32/64-bit) modes for DMA other than bit-planes - Audio, Floppy,

3) Addition of BPU/RGA override bits to support interleaved bitplane and chunky pixel modes.

4) Addition of "REPLAY" control line to support video decompression.

## Phase 2 Architectural Enhancments

### Previously defined:

1) Chunk Pixel Modes (2/4/8 bit, Dual Playfield 2/4).

2) Interleaved Bit Plane (Atari) Mode.

3) Robbins Color Table Additive HAM (SLAM).

4) 16/24-bit True Color / Direct Video.

5) Recycling sprites.

6) Hi-res monochrome (1280*1024, 2 bitplane support).

### New/Revised:

1) Fast Color table load - multiple copper or "bitplane".

2) Sprite/Floppy/Audio "foldback" for improved 70 Hz.

3) Enhanced "HAM" replacement - computational/blend/luma-chroma.

4) CD/I level video decompression for full motion video.

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